REMARKS

In the Office Action the Examiner rejected all claims 1, 4, 6, and 8-15 under 35 U.S.C. 102 as being anticipated. Claims 1, 4, 6, and 8-15 remain under examination.

The Examiner referenced reasons provided in the rejection of 12/1/05 and provided additional comments with respect to applicants' response to the rejection of 12/1/05 as to why Weiberneit anticipated applicants' claims.

The Examiner stated that a distinction pointed out by applicants was "merely the intended use of the applicant's invention and therefore cannot be relied upon to define over the prior art." The distinction in question relates to the first and second input signals being in the same logic state during the second clock state. Applicants disagree that this distinction from Weiberneit is merely an intended use. It's an actual use described in the specification that is important to the successful operation of the circuit. The second clock state is the time when transistor 226 is active which is the time when the inverters 220 and 230 are providing the latching function. If the input signals were not in the same logic state, logic low in the described embodiment, then one of the input signals would be in the logic high state. Thus, for example, if the DATA signal were a logic high, transistor 202 would be conductive and would be attempting to bring the first node to a logic low which would have the effect of forcing DOUT to a logic high. This would defeat the purpose of the latch of inverters 220 and 230 which is intended for sustaining a particular logic state for DOUT and DOUTB during the second clock state. Accordingly, applicants believe that the claiming of this feature is material and is not just to purpose, especially with regard to independent claims 1 and 6, which are method claims.

The Examiner further pointed out that applicants admitted in the specification that it is prior art to have complementary signals forced to the same logic state. Of course that is known in certain situations but not in this combination as claimed. Virtually all patentable inventions are combinations of things known in the prior art, whether it be method or apparatus. Applicants described that it is known that complementary signals can also be the same logic state in some situations. That is far different from saying that providing the complementary signals in the same logic state during the second clock state is not a material feature in the combination of elements that make up the claims. Thus, applicants submit that the characterization in the specification referenced by the Examiner cannot properly be used for the purpose of asserting

that this claim limitation is not a material limitation and accordingly that that this limitation cannot be ignored.

This Office Action and the referenced Office Action of 12/01/05 contained numerous statements characterizing the claims, the specification, and the prior art. Regardless of whether such statements are addressed by applicants, applicants refuse to subscribe to any of these statements, unless expressly indicated by applicants.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning the current application.

Respectfully submitted,

SEND CORRESPONDENCE TO:

By: James L. Clingan Jr

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

James L. Clingan, Jr
Attorney of Record
Reg. No.: 30,163
Telephone: (512) 996-6839
Fax No.: (512) 996-6854